# DESIGN AND OPTIMIZATION OF 4-BIT ARRAY MULTIPLIER WITH ADIABATIC LOGIC USING 65 NM CMOS TECHNOLOGIES

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**Abstract:** This paper proposes a 4-bit array multiplier useful in the design of basically mixer circuit, which is highly involved in signal and image processing using an efficient low-power VLSI technique. The presented architecture is completely implemented adiabatic techniques in the Near Threshold Region, which optimize the product of propagation delay and power dissipation. Multiplier is the most frequently used element in many digital electronics applications. Depending on the applications, various types of multipliers emerge. With this technique, the total power dissipation, i.e. dynamic power dissipation as well as static power dissipation is less as compared to the conventional CMOS technique. The Near Threshold Adiabatic Logic (NTAL) technique is used with a single time varying power supply which reduces the clock tree management and enhances the energy-saving capability. Simulation of the proposed design is done by Tanner tools schematic editor with wedit simulator on TSMC 65nm technology node to verify the optimized result.

**Index Terms:** Near Threshold Adiabatic Logic, Adiabatic, CMOS Multiplier, efficiency, Power leakage.



**Introduction:** VLSI technology facilitates the designers for embedding more than hundred thousand of gates in a single IC. Achieving power reduction in full adder circuits is essential in handheld and portable VLSI based application circuits. Most of these application cir- cuits incorporate processor-based blocks. For example, microprocessor [1] , digital signal processors, digital image processors, cryptographic processors [2] , etc. In each one of these processors, arithmetic and logic units with multipliers, dividers, modulators, logarithmic amplifiers, memories, etc., will be the major blocks. Most probably, the circuits inside these blocks have full adder as their main element [3] . Hence, in order to obtain the overall power optimization in a VLSI IC, as an initial attempt, the power reduction in full adders is the prime aim of the VLSI designers [4] . Observing the design with higher levels of abstraction, namely algorithmic and architectural levels for each subcircuit of a VLSI IC, leads to increased complexity. Representing the needed subcircuits in any one of the convenient lower levels of abstraction, namely circuit, logic, and transistor levels are done with ease with the help of the instruction formats. Thus, in order to have an efficient approach, that is to implement the application circuits inside the VLSI IC provide many choices for describing, synthesizing and verifying the designs with reduced complexity. Depletion of the silicon area during fabrication leads to the de- cline in power consumption.

Thus, choosing low power consuming logic styles in the logical design stage and improving the efficiency of the physical design stage by adopting enhanced place- ment and routing techniques will yield a low power design with reduced propagation delay. With this perception, the design and implementation of a low power full adder cell were carried out by selecting the low power consuming logic styles such as CMOS based 28T full adder cell [5] , PTL based 16T full adder cell with TG, PTL based 14T full adder cell with TG and proposed ALFAcell. In VLSI, there is a trade offbetween area, power and delay. To overcome these issues, it is necessary to design an optimized de- sign. Hence the ALFA cell is proposed that overcomes the problems of the existing techniques such as CMOS Full Adder, PTL logic and transmission gate. Low power consumption is required to optimize battery back-up in digital devices, to ensure stable and optimum working of circuit and also for longer device life. In existing CMOS technologies sub threshold leakage current is larger than other leakage components. As technology scales down to nano meter, sub thresh- old leakage power increases exponentially with the reduction of supply voltage. Minimizing leakage power is an important task in portable devices to increase the battery life. Many techniques have been proposed for designing VLSI circuits with low power. The proposed techniques CMOS, MTCMOS and MTNCL are effective techniques to reduce power consumption. These logics can provide high speed and low power designs. In this paper, Multiplexer is de- signed with proposed techniques and simulation results are com- pared with existing techniques. Motivated by the emerging battery operated hand-held devices, minimizing energy consumption has become a significant concern in the semiconductor industry. On the other hand, heat generation in largescale computing systems has become a severe challenge. In recent years, some techniques were introduced to reduce the energy consumption and heat generation in computing devices. These methods were proposed with the aim of reducing energy consumption due to both the dynamic activities and leakage issues. Generally, in previous decades, the dynamic energy consumption was the dominant factor in the battery depletion [1]; but in recent years, due to the enormous amount of progress in the scale of technology, the leakage energy has also become very critical [1]. The previous efforts on mitigating the dynamic energy consumption in digital circuits are extensive. Meanwhile, the *charge recovery* is a promising approach which tries to reduce the power consumption significantly [2]. In several circuit-level implementations of the charge recovery, reversible patterns (which are compliant with Landauer's principle [3]) have shown less energy consumption [4–10]. According to the Landauer's principle, losing any bit would lead into dissipation of energy with a size of $kTln(2)$, where $k$ is the Boltzmann's constant while the $T$ is indicating the temperature [3,11,12]. Therefore, to reduce energy consumption, information should not be erased. Any logic operations, which does not require erasing information is called a reversible logic operation [3]. Adiabatic circuits are based on reversible logic [12,13]. In adiabatic circuits, two significant changes have reduced dynamic energy consumption. The first reason is the use of constant current for charging the output capacitors. This constant current in such circuits is generated through a ramp voltage source. The ramp voltage can minimize the potential difference between drain and source terminals; Hence, it could

reduce the energy consumption during switching phases. The second is the power supply features that are capable of recovering energy stored in the output capacitors and preventing their dissipation. Although adiabatic circuits reduce the dynamic energy consumption, some methods have been also developed to reduce leakage in adiabatic circuits. These methods use variable capacitors instead of transistors, thereby reducing leakage [14–17]. These studies have used NEMS (Nano Electro Mechanical Systems) instead of CMOS (Complementary Metal Oxide Semiconductor) in adiabatic circuits to reduce the static energy. On the other hand, one of the unexplored characteristics of adiabatic families, is their inherent hardware redundancy [4–10]. Therefore, in addition to their energy efficient structure, adiabatic circuits are potentially more resilient to faults in comparison with classic circuits. To the best of our knowledge, although there have been many studies on the concept of energy recovery and mitigating energy consumption in adiabatic circuits, there have not been any efforts on exploiting their resistance to faults to provide more reliable computing devices. On the other hand, adiabatic circuits are used to improve hardware security.

**Literature Survey:** Advanced designer's present-day face two fundamental difficulties in the mapping of DSP calculations to silicon are planned multifaceted nature and power productivity. Power/vitality proficiency can be just sent by acknowledging of the entry ways and diminishing the supply voltage, exchanged that the engineering meets accomplishment and region stipulations. Door investigation is a notable issue and can be deteriorated from top coordinated down to the basic information way rationale. The utilization of worldwide Vdd scaling to improve capacity requires reasonable rationale profundity which requires retiming at the miniaturized scale building level. Hierarchic plan of macros into structure engineering may need added pipeline tuning to boost generally speaking productivity. Pipelines is a critical advance in have worldwide optimality. Another undertaking is to expand zone (cost) productivity, which requires dynamic equipment set. The creating multifaceted nature of advanced frameworks further underscores the requirement for robotized engineering investigation. Customarily, engineering configuration has been an interrogative procedure including numerous cycles before the last plan joins to wanted particulars. There is a technique for computerizing the procedure of design determination for superior and vitality touchy frameworks. The ideal models meet framework necessities for power, region, and throughput while using the characteristic computational productivity of the hidden innovation [1]. The multiplier is an essential portion of (DSP) in light of the fact that it generally decides the accomplishment of the chips. As a result of huge circuit unpredictability, the power utilization and the format region are another two plan discourses of the multiplier. In-depth analysis of the adiabatic logic's behaviour in the near threshold domain has been done in this section. One sinusoidal power source is all that is needed for the Near Threshold Adiabatic Logic (NTAL) style to operate well, which simplifies clock tree maintenance and increases energy efficiency [1]. Here, specific information on NTAL circuits' power dissipation, voltage swing, influence of load, temperature, frequency, etc. is provided [2]. The

effectiveness of the suggested approach has been validated using extensive Cadence simulations at the TSMC 65nm technology node [3]. To drive the intricate NTAL circuits, a power clock has been created based on a switched capacitor regulator [4]. High degree of agreement between analytical and simulated data verifies the suggested adiabatic logic style in the near threshold domain [5]. The number of transistors in a chip has multiplied over the past several decades, enabling a wide range of computer applications, but power budgets are restricting the usefulness of these transistors. Subthreshold operation has emerged as a viable solution for power reduction. By adding subthreshold operations, where the supply voltage scales down below the threshold voltage of the metal oxide semiconductor field effect transistor (MOSFET), researchers have attained the goal. Subthreshold logic [6] functioning was severely constrained by lower energy efficiency, an exponential rise in leakage power, sensitivity to noise, unfavorable features, etc. It has been discovered that adiabatic logic is useful forobtaining low power in VLSI designs. The circuit carries little current and uses less power at the subthreshold zone. In this research, subthreshold adiabatic logic has been implemented using a dual rail power supply with a 0° and 180° phase difference (SAL) [7].

**PROPOSED METHOD:**

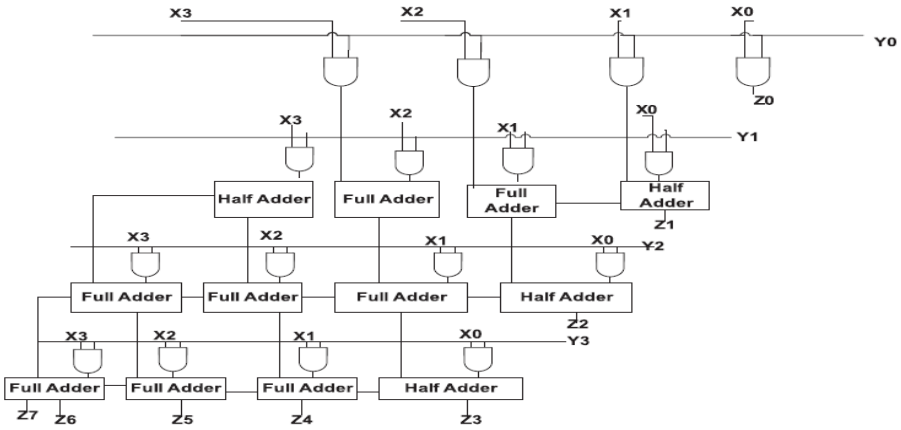


**Figure:1** Logic diagram of NTAL 4-bit Array Multiplier

Most digital multipliers operate on the utmost fundamental uses of multiplication, which is accomplished through a series of bit shift and bit addition operations. The final output is combination of both the factor of multiplier that is a multiplier and a multiplicand. Now a days, numerous types of multipliers are used in digital circuits and based on different technology, but some of them are more power consuming. The frequently used multiplier in signal processing is array multiplier with less power consumption. In this paper, the 4-bit

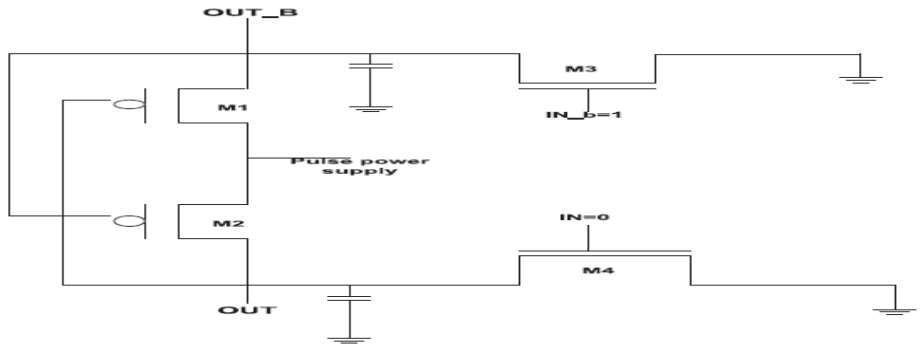


**Figure 2:** Basic circuit diagram of Near Threshold Adiabatic Logic (NTAL) inverter

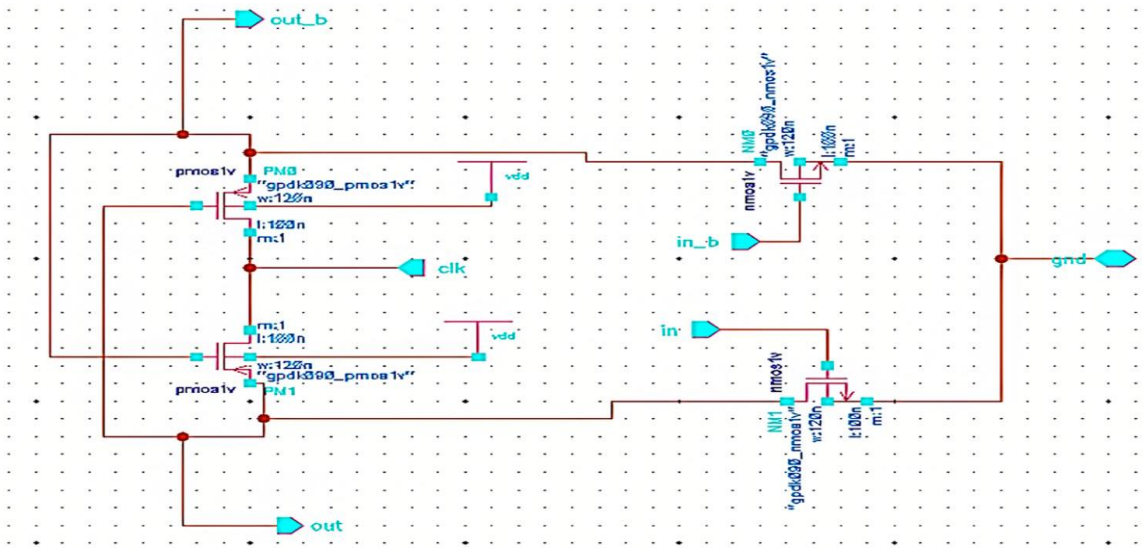


**Figure3:** Schematic diagram of basic building block of proposed NTAL inverter

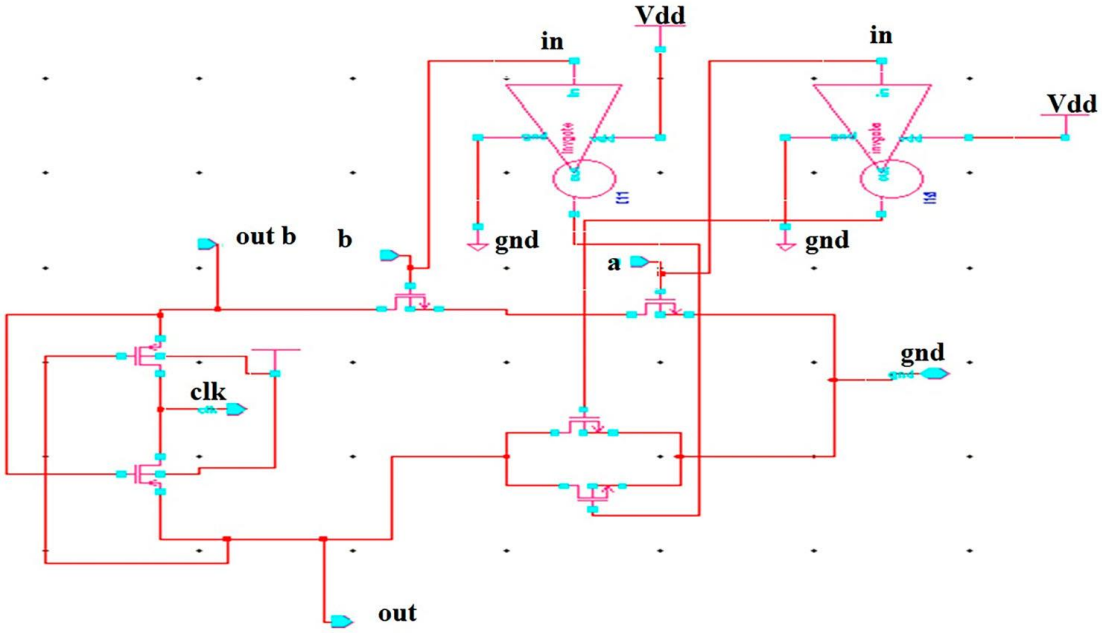


**Figure 4:** Schematic diagram of basic building block of proposed AND/NAND using NTAL

array multiplier is discussed with implementation using NTAL Logics . The basic algorithm for NXN multiplication required *N* bit multiplicand by *N*-bitmultiplier as given in Equations
(1) and (2).

$Y = Yn-1Yn-2Yn-3 \ldots Y4Y3Y2Y1Y0$ Multiplicand (1)

$X = Xn-1Xn-2Xn-3 \ldots X4X3X2X1X0$ Multiplier (2)

The array multiplier is well known in various applications of digital signal processing due to its regular structure. Multiplier circuit consisting of the AND gate for partial products and half, full adder for addition and summation of internal product terms . If any multiplier has *N*-bit multiplicand and *M*-bit multiplier then product term is represented as $N*M$ partial product

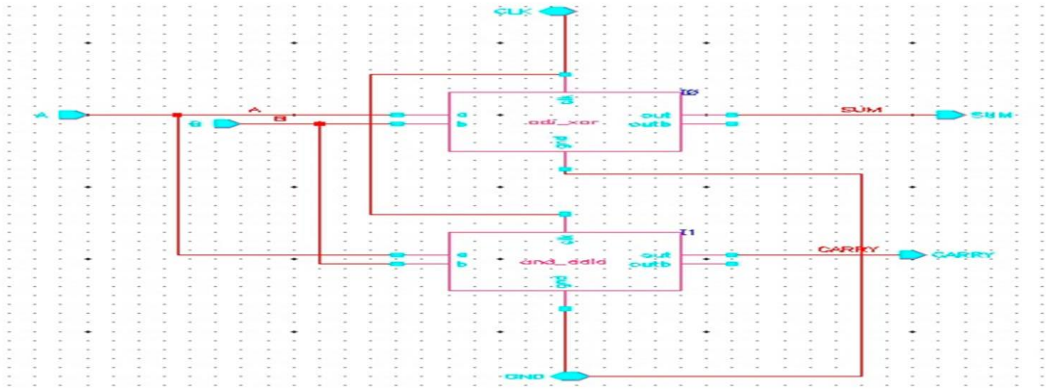


**Figure 5** Schematic diagram of proposed Half Adder using NTAL

and the product term is generated or summed up using
Equation (3).

$$P(m+n) = A(m)B(n) = \sum_{i=0}^{m-1}\sum_{j=0}^{n-1} a_i b_j 2^{i+j}$$

Implementation of Inverter/Buffer AND/NAND Gate, OR/NOR Gate using the NTAL: one array multiplier needed implementation of Inverter circuit, AND/NAND gates, half adder and full adder circuits.

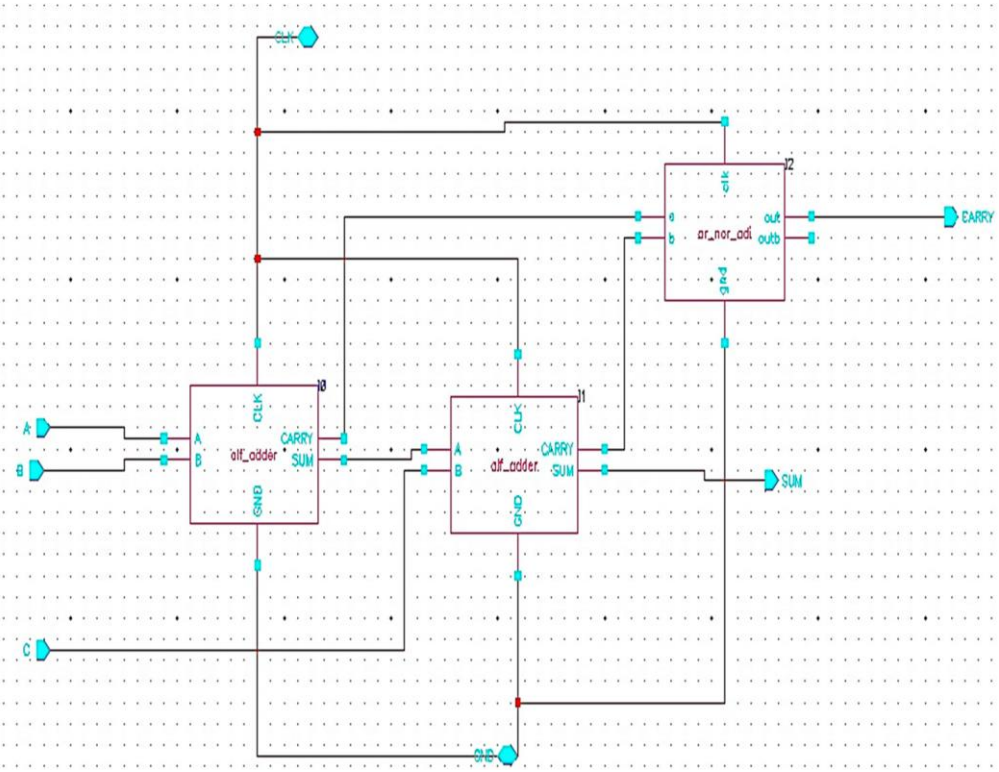


**Figure:6** Schematic design basic building block of proposed Full Adder using NTAL

AND/NAND Gate using NTAL logics and give the satisfactory results for power dissipation [39]. Implementation of half adder and full adder using NTAL: In this Section 1, bit half adder is implemented using the said technology and simulated with the Boolean expression [40]. If A andBare two binary inputs then sum(*S*) in Equation (2) and carry (*C*) in Equation (3) are define as

$S = A \oplus B$ (4)

$C = A \cdot B$ (5)

A 2-bit ripple carry adder is created and simulated to show how adiabatic logic and near-threshold operation operate. The half-adder used in the ripple carry adder can be implemented using XOR and NAND gates. Figure 5 depicts the ripple carry adder's schematic. Efficient Charge Recovery Logic implements the sum and carry parts of a complete adder. The schematic diagram of half adder is shown in Figure 5 and simulated waveformis depicted in Figure 6. Virtuoso Simulator is used to implement the entire design, and simulations can verify the circuit's operation. The supply voltage in the experiment is set at 0.65V, which is a little higher than the absolute value of the PMOS threshold voltage (0.423 V).We modified the peak-peak voltage to 0.7 and 1.0V, respectively, to examine the energy consumption of circuits operating at different voltage regions as shown in Figure 6. Similarly, 2-bit full adder using Double Pass Transistor (DPL) and multi-output carry look-ahead logic (CLA) is also implemented and simulated in Figures 7 and 8 using NTAL technology by cascading the two-half adder circuit and Gates, which perform satisfactory results. Simulation parameter is similar to the half adder

circuit mentioned above. Implementation of proposed 4-bit array Multiplier: For implementation of NXN array multiplier, it required AND gates for computing the partial product and for the terms summed it required N half adder and N(N-2) full adder as shown in Figure 9. The proposed architecture of 4-Bit array Multipliers required 16 AND gates, 4 half adder, and 8 full adders. The circuit implementation and simulation of the proposed architecture of 4-bit Array Multiplier is done using Cadence Virtuoso schematic tools. Schematic diagram cannot be fitted in this paper size so simulated waveform of proposed multiplier with all inputs detail is shown in Figure. Simulation is tested with the input signal first

X [3:0] = 1010 and Y

[3:0] = 1010. After the simulation, the output is calculated

at Z [7:0]. The calculated output for the applied input is expected as

Z [7:0] = 01100100.

completed the check of functionality of proposed architecture of 4-bit array multiplier and gives the satisfactory results. All results of full adder and half adder are compared with available CMOS implementation in Ref. [23]. In order to confirm the resilience of half-adder and full-adder configuration operating in near-threshold regime, process variations are taken into consideration in the design. On the basis of 65nm CMOS technology, all tests are presented [10], and the pertinent process changes are explained [17]. The three main sources of process variation are length, threshold voltage, and mobility.

**RESULTS:**

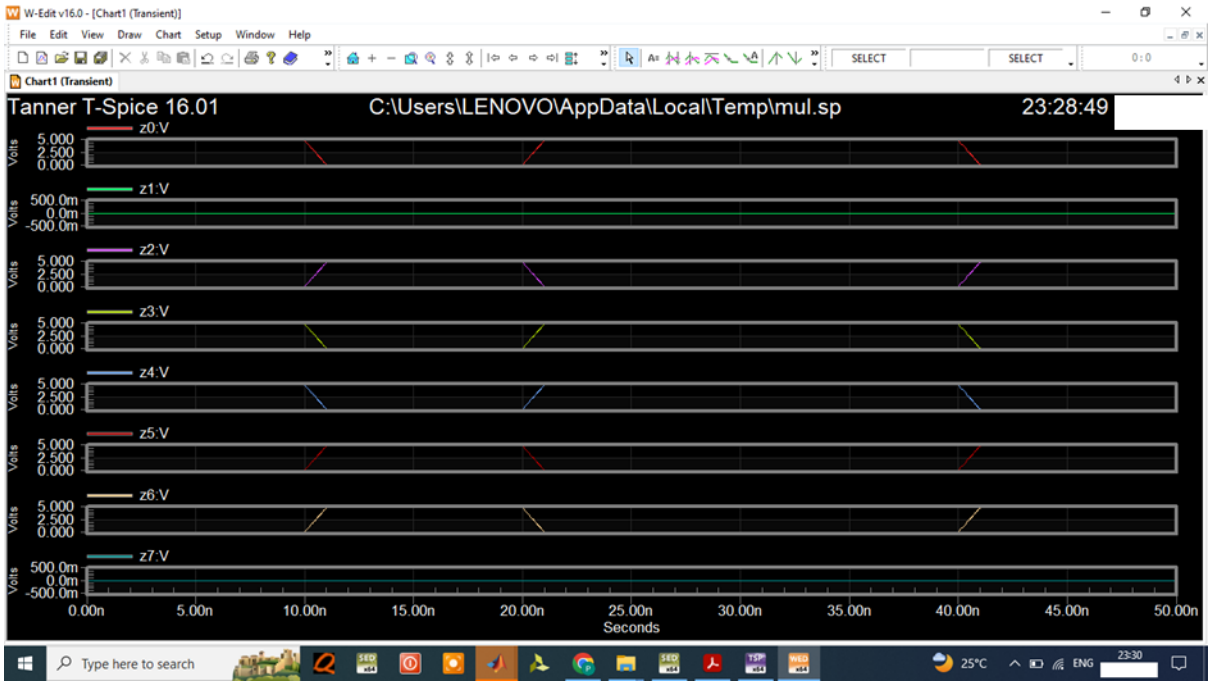


**Fig a: Proposed Simulation Results**

**CONCLUSION:** In this paper, the most suitable technique Near Threshold Adiabatic Logic (NTAL) technology is proposed and compared with CMOS technology for the digital application circuit 4-bit array multiplier. After reviewing all types of adiabatic techniques, it was observed that the NTAL design method is most appropriate for digital signal solutions because of the low power execution. The NTAL design method is found to be superior for logic circuits than the more traditional CMOS design technique in terms of power dissipation but complex in terms of circuit execution.

**FUTURE SCOPE:** The above proposed methodology can be adopted to future optimization base image processing methods which may present a better system.

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