ENERGY EFFICIENT SECURE MEMORY ELEMENTS IN DIGITAL DEVICES

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ABSTRACT:

Low complexity turbo-like codes based on simple two-state trellis or simple graph structure results in encoding with low complexity. Out of this Convolution encoder and turbo codes are widely used due to the excellent error control performance. The most popular communications encoding algorithm, the iterative decoding requires an exponential increase in hardware complexity to achieve greater encode accuracy. This project focuses on the realization of turbo encoder and decoder using Log-Map based Iterative decoding technique.The turbo codes are designed with the help of Recursive Systematic Convolutional and are separated by inter leaver, which (component used to rearrange the bit sequence) plays a vital role in the encoding process. This paper provides the design of a Turbo Encoder, which is parallel concatenation of Recursive Systematic Convolutional (RSC) encoders and inter leaver to reduce delay. The Turbo Encoder is designed by Verilog-HDL and Synthesized by Xilinx ISE.

Keywords: Encoder system, Recursive Systematic Convolution, Error control performance.

INTRODUCTION

Error could be a condition once the output information doesn't match with the input information [1]. Throughout transmission, digital signals suffer from noise which will introduce errors within the binary bits movement from one system to another. That means a 0 bit might change to 1 or a 1 bit might change to 0. Whenever a message is transmitted, it might get push by noise or data may get corrupted [8]. To avoid this, we use error-detecting codes which are additional data added to a given digital message to help us detect if an error occurred throughout transmission of the message. A straight forward example of error-detecting code is parity check. Along with error-detecting code, we are able to pass some data to work out the original message from the corrupt message that we received [3]. This type of code is termed as an error-correcting code. Error-correcting codes also deploy the similar strategy as error-detecting codes however in addition; such codes also detect the exact location of the corrupt bit. In error-correcting codes, parity check encompasses an easy way to detect errors along with a sophisticated mechanism to work out the corrupt bit location. Once the corrupt bit is found, its value is reverted (from zero to one or one to zero) to urge the original message. To detect

and correct the errors, extra bits are super imposed to the data bits at the time of transmission. The extra bits are referred to as parity bits [7]. They permit detection or correction of the errors. The data bits in conjunction with the parity bits form a code word. Parity checking is employed for error detection. It is the best technique for detecting and correcting errors. The MSB of an 8-bits word is employed as the parity bit and the remaining 7 bits are employed as data or message bits. The parity of 8-bits transmitted word is either even parity or odd parity. Even parity suggests that the amount of 1's within the given word as well as the parity bit should be even (2, 4, 6 ...). Odd parity means the number of 1's in the given word including the parity bit should be odd (1, 3, 5 ...). The parity bit is set to zero and one depending on the type of the parity needed [10]. For even parity, this bit is set to one or zero such that the no. of "1 bits" in the entire word is even. For odd parity, this bit is set to one or zero such that the no. of "1 bits" in the entire word is odd.The theory of error-correcting codes was originated in the late 1940's by Richard Hamming, a mathematician who worked for Bell Telephone. Hamming's motivation was to program a computer to correct "bugs" which arose in punch-card programs. Hamming's overall motivation behind the theory of error-orrecting codes was to reliably enable digital communication.

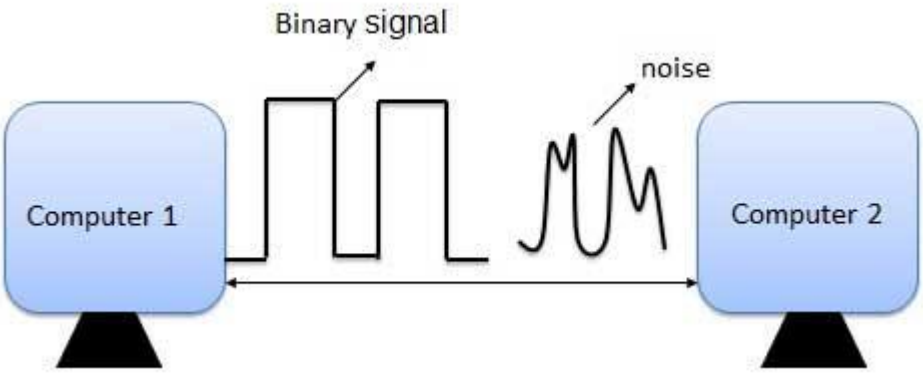
LITERATURE SURVEY

Turbo code is a parallel concatenation of two convolutional codes separated by a random interleaver. It is near channel capacity error correcting code. This error correcting code is able to transmit information across the channel with an arbitrary low bit error rate (Proakis 1995). It has been shown that a Turbo code can achieve performance within 1 dB of channel capacity (Berrou et al 1993). Random coding of long block lengths may also perform close to channel capacity, but this code is very hard to decode due to the lack of code structure. The performance of a Turbo code is partly due to the random interleaver used to give the Turbo code a "random" appearance. 15 However, one big advantage of a Turbo code is that there is enough code structure to decode it efficiently. There are two primary decoding strategies for Turbo codes. They are based on a maximum aposteriori probability algorithm and a soft output Viterbi algorithm. Regardless of which algorithm is implemented, the Turbo code decoder requires the use of two (same algorithm) component decoders that operate in an iterative manner. Various research groups working with Turbo codes around the globe are Caltech Communications Group, California Institute of Technology, USA, Coding Research Group, University of Hawai at Monoa, USA, Coding Research Group, University of Notre Dame, USA, Communications Group, Politecnico di Torino, Italy, Communications Laboratory, Technion - Israel Institute of Technology, Israel, Communications Laboratory, TechnischeUniversität Dresden, Germany, Communications Research Centre, Canada, Communications Research Group, University of York,

United Kingdom, Communications Research in Signal Processing, Cornell University, USA, Communications Systems and Research Section, Jet Propulsion Laboratory, USA, Complex2Real, Turbo Code Tutorials, USA, Comtech AHA, USA, DataLab, University of California, Irvine, USA, David J.C. MacKay, Cambridge University, United Kingdom, DSP Derby, India, Efficient Channel Coding, USA, eritek, USA, Error Correcting Codes Home Page, Japan, Flarion Technologies, USA, iCODING Technology Incorporated, USA, Institute for Communications Engineering, TechnischeUniversitätMünchen, Germany, Institute for Telecommunications Research, University of South Australia, International Symposium on Turbo Codes, ENST de Bretagne, France, Iterative Connections, Australia, Iterative Solutions, USA, Jakob Dahl Andersen, Technical University of Denmark, Lei Wei's, University of Central Florida, Orlando, USA, Mobile Multimedia Research, University of Southampton, United Kingdom. Patrick Robertson, DeutschesZentrumfürLuft-und Raumfahrt (DLR), Germany, Small World Communications, 16 Australia, Telecommunications Laboratory, University Erlangen-Nürnberg, Germany, Turbo Codes at West Virginia University, West Virginia University, USA, Turbo Codes in CCSR, University of Surrey, United Kingdom, Turbo Concept, France, VLSI Digital Signal Processing Laboratory, University of Minnesota, USA, What a wonderful Turbo world, Australia, Wireless Systems Laboratory, Georgia Institute of Technology, USA, Xenotran, USA, etc. This Chapter gives a summary of Turbo codes and considers the related research efforts concerned to Turbo code. It also explains performance of modified SOVA and modified log MAP.

ERROR DETECTION AND CORRECTION TECHNIQUE

Error is a condition when the output information does not match with the input information. During transmission, digital signals suffer from noise that can introduce errors in the binary bits travelling from one system to other. That means a 0 bit may change to 1 or a 1 bit may change to 0.



Error-Detecting codes

Whenever a message is transmitted, it may get scrambled by noise or data may get corrupted. To avoid this, we use error-detecting codes which are additional data added to a given digital message to help us detect if an error occurred during transmission of the message. A simple example of error-detecting code is **parity check**.

Error-Correcting codes

Along with error-detecting code, we can also pass some data to figure out the original message from the corrupt message that we received. This type of code is called an error-correcting code. Error-correcting codes also deploy the same strategy as error-detecting codes but additionally, such codes also detect the exact location of the corrupt bit.

In error-correcting codes, parity check has a simple way to detect errors along with a sophisticated mechanism to determine the corrupt bit location. Once the corrupt bit is located, its value is reverted (from 0 to 1 or 1 to 0) to get the original message.

How to Detect and Correct Errors?

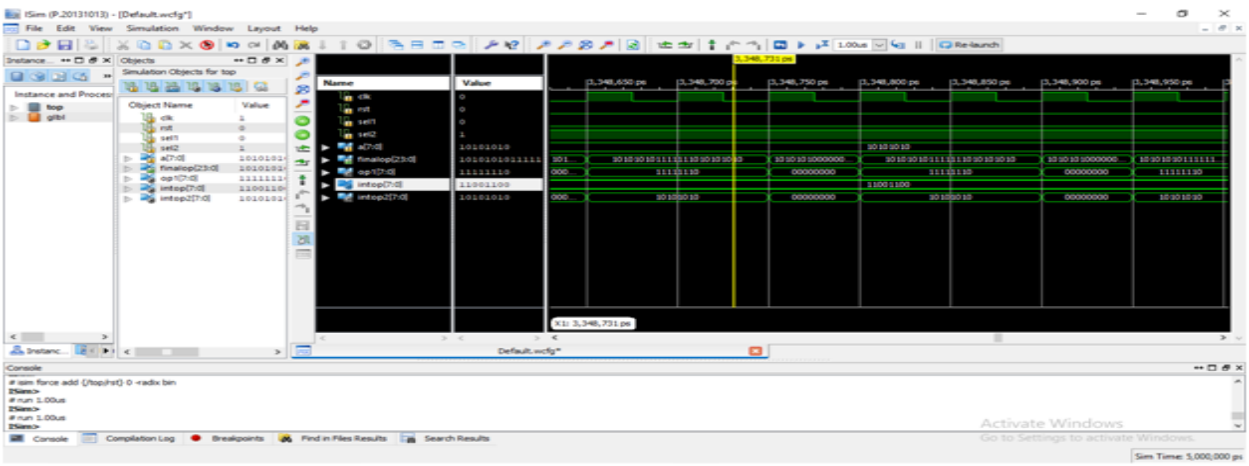
To detect and correct the errors, additional bits are added to the data bits at the time of transmission.

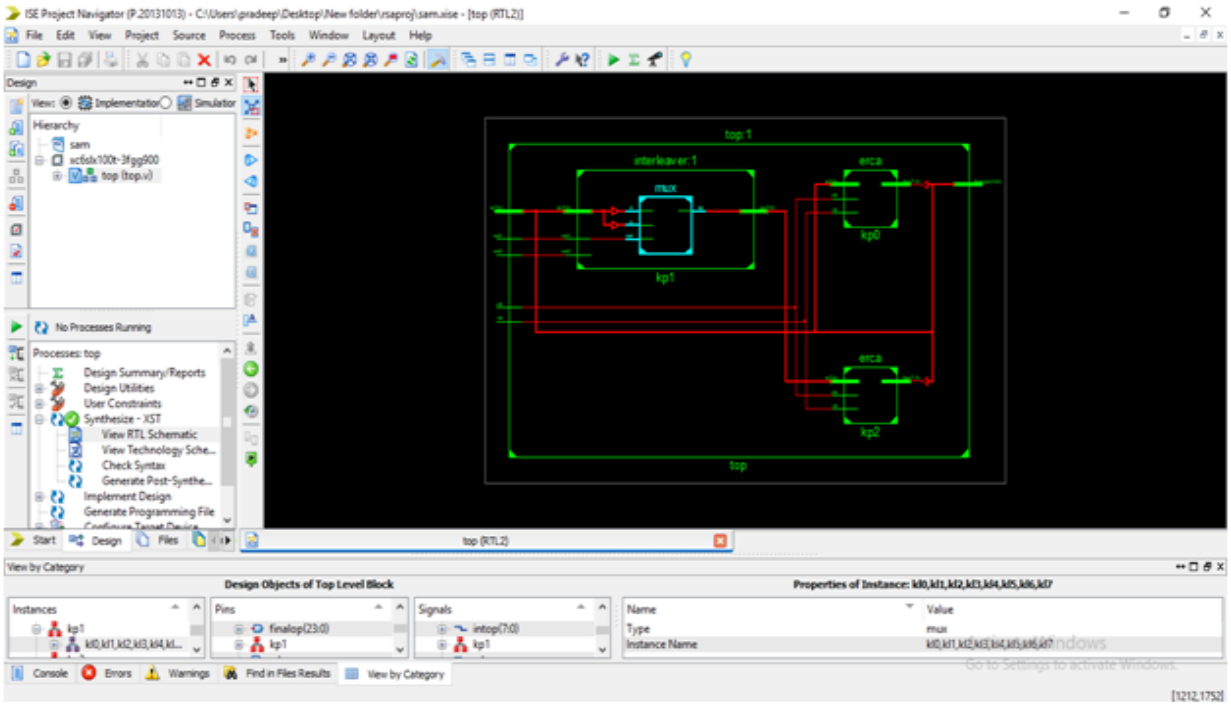
- The additional bits are called **parity bits**. They allow detection or correction of the errors.
- The data bits along with the parity bits form a **code word**.

Parity Checking of Error Detection

It is the simplest technique for detecting and correcting errors. The MSB of an 8-bits word is used as the parity bit and the remaining 7 bits are used as data or message bits. The parity of 8-bits transmitted word can be either even parity or odd parity.

SIMULATION RESULTS





CONCLUSION

The Turbo Encoder is designed using Verilog-HDL and simulated using Xilinx ISE 14.7, by considering 8-bit input stream and 16-bit input stream. It is observed through the simulation results that the Turbo Encoder with 8-bit input is more efficient when compare with existing methodologies. These parameters can have negative effects when very low BERs are simulated. Another cause for the limitation in BER performance is a poor interleaver design. Due to highly correlated sequences, the BER decreases to a certain level from the decoding process. SO, interleaver is designed in efficient manner.

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