DESIGN OF A LOW-POWER COMPACT CMOS VARIABLE GAIN AMPLIFIER FOR MODERN RF RECEIVERS

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ABSTRACT
The requirements for portability have required rapid development of low power electronic communication products. The variable gain amplifier (VGA) is one of the weakest components of any modern receiver in terms of a correct signal baseband processing. Most CMOS VGAs have low bandwidth and limited gain range. In this paper, two stage class AB VGA consisting of direct transconductance amplifier and linear transimpedance amplifier is designed in Silterra 0.13-µm CMOS technology using Mentor Graphics environment. According to the post-layout simulation findings, the VGA design achieves the highest gain range of -33 to 32 dB and the broadest bandwidth of >200 MHz. The VGA merely uses 2 milliwatts of power. a single DC 1.2 V source. The core chip area of the VGA is likewise only 0.026 mm2 which is also the lowest compared to current researches. For all contemporary communication gadgets, such a VGA will be a very helpful module.

Keywords:CMOS, Receiver, RF, VGA

I INTRODUCTION

Scientists are compelled to create extremely small and power-efficient communication gear due to the need for portability and affordability [1-3]. The constant improvement in CMOS technology made the realization of fabricating fully integrated receivers easy maintaining the maximumperformance. RFID, Bluetooth, Zigbee, Wi-Fi, and WLAN devices are examples of low-power, portable, and inexpensive RF communication devices that are now accessible [4–8]. One of the components of a receiver that is most susceptible to improper baseband signal processing is the variable gain amplifier [9–10]. Regardless of the actual signal strength collected by the antenna, the VGA is typically used in communication RF receivers to stabilize the signal processed by the baseband circuitry [11–14].VGA must function with low power supply voltage [15–16] and low power consumption [17–18] in portable communication devices.

Devices with low supply voltages are made possible by advancements in process technology. Consequently, the majority of low power integrated circuits use voltages of the power supply that are lower than 1.2 V. At low supply voltages, designing a CMOS VGA that is low power, wide bandwidth, and extremely linear is essential [19–20]. A typical RF receiver front-end with a variable gain amplifier is depicted in Figure 1. The VGA circuitry can be realized in two different ways. The first one creates discrete gain steps by adjusting between different passive feedback sources using a switching mechanism. It is frequently referred to as digitallymanaged VGA.

Analog gain control signal regulates an adjustable transconductance or resistance of the second kind, which is analog linear-in-dB. Each of the architectures has pros and cons of its own [21–22]. It is commonly recognized that distortion can be minimized by using negative feedback. given the availability of linear feedback components. Usually, only passive components satisfy the requirements for linearity. Consequently, passive feedback elements must be selectively switched into the signal channel in order to be used in a VGA. Although the separate gain levels may be a drawback for certain receivers, these circuits can nevertheless achieve respectable linearity for high output voltages because they can take use of negative feedback. In wireless communication systems, for instance, the signal phase ought to be continuous. Consequently, the discrete gain step VGA is not recommended [23–24].

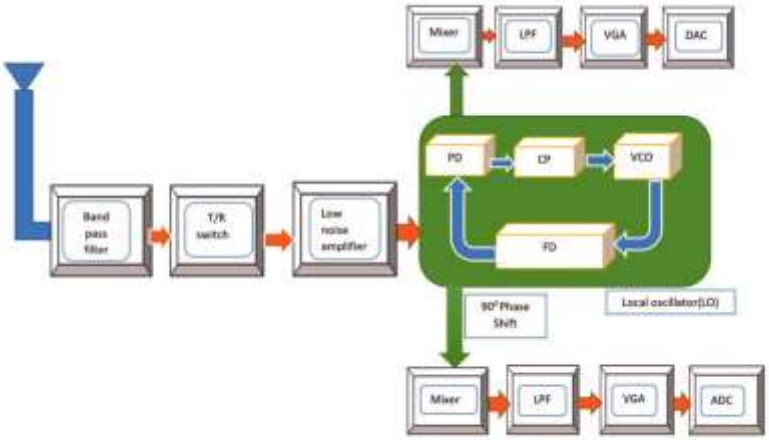


Figure 1. A typical RF receiver front-end

One or more circuit parameters, such as the bias voltage or current, can be continually changed to obtain continuous control of the gain. These circuits have the benefit of gently varying the gain between extreme extremes. The linearity of such an amplifier is a drawback is usually inadequate. Maintaining low signal levels is the only method to obtain acceptable distortion performance since changing the bias point of an intrinsically nonlinear device changes the gain. Several VGA circuit architectures, including pseudo-exponential function, quasi-exponential function, current steering, feedback tuning, and Cherry-Hooper VGA, have been presented by researchers based on the control mechanism, which is the main problem in analog VGA design.

To achieve particular performance requirements, some designs have been modified and additional circuits have been added [25–26]. Nonlinearity, poor gain, narrow bandwidth, and excessive power dissipation have plagued the majority of them. Therefore, for low-power communication devices, a highly compact VGA design with improved performance is crucial. The design of a two-stage low power, broad bandwidth, and compact class AB variable gain amplifier in the Silterra 0.13 µm CMOS technology is demonstrated in this study. The limited bandwidth and gain range at low supply voltages at a very small device are overcome by the suggested VGA.

II LITERATURE SURVEY

A comparative study of CMOS mixer topologies based on the Gilbert cell design for RF front-end communication systems was given by Khan et al. in 2017. The study was mostly mixer-focused and not directly applicable to variable gain amplifier (VGA) design, despite the fact that it offered helpful insights into mixer performance. In 2018, Santos et al. suggested a programmable gain amplifier combining active negative resistance and replica biasing techniques aimed at ultra-low-power biomedical and sensor interface applications; however, the device suffered from low unity-gain frequency and limited scalability for RF applications. A DTMOS-based VGA using OTA cascaded current mirrors with Miller compensation was presented by Panchal et al. in 2019 for low-power analog signal processing. However, the method was only applicable to kHz-range bandwidth and was not appropriate for high-frequency RF systems.Targeting wireless and portable RF systems, Ramakrishna et al. created an inductor-less low-noise amplifier in 2020 utilizing a mix of common-gate and common-source stages with body biasing. However, the design had a restricted gain-tuning range and mediocre noise performance. For 2.4-GHz IoT and WLAN applications, Ceolin et al. introduced an ultra-low-voltage inverter-based LNA with forward bulk biasing in 2021. Although it operated at low voltage, its power consumption was more than that of newly developed nanowatt-level devices. For mm-wave and V-band RF communication systems, Moody et al. most recently proposed a V-band LNA in 2022 using inductive source degeneration and current-reuse techniques. However, the design complexity and increased chip space caused by inductors remained major obstacles.

III EXISTING SYSTEM

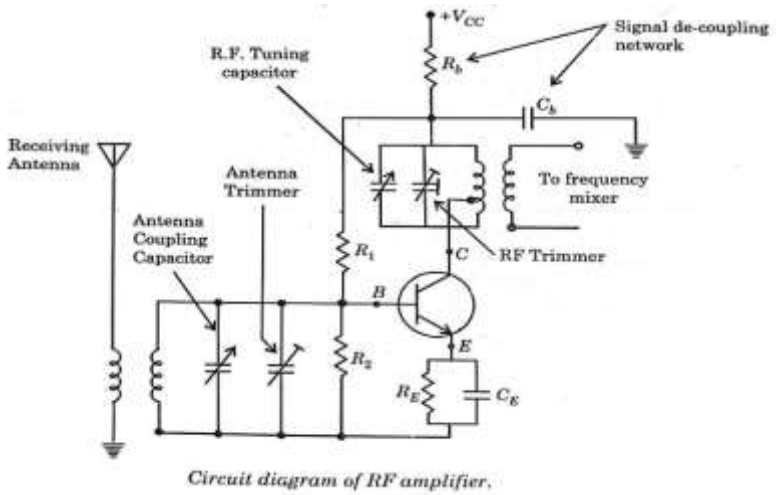
An RF (Radio Frequency) amplifier used in the current (conventional) superheterodyne radio receiver system is seen in the diagram. It is situated immediately after the receiving antenna and before the frequency mixer. This stage's primary job is to reject undesired signals and noise while selecting and amplifying the intended RF signal. Antenna Coupling Network and Receiving Antenna:

Electromagnetic waves from the atmosphere are captured by the receiving antenna and transformed into a faint radio frequency electrical signal. The antenna coupling capacitor, which only permits the RF signal to flow while blocking DC, is used to feed this signal to the RF amplifier. The coupling ensures adequate impedance matching between the antenna and the tuned circuit, enhancing signal transfer and lowering signal loss.
RF tuning circuit with antenna trimmer:
Together with the inductor, the antenna trimmer and RF tuning capacitor provide a tuned LC circuit. Selectivity, or allowing only the chosen frequency band to pass while rejecting other frequencies, is the function of this circuit. The receiver can be tuned to various radio stations by varying the RF tuning capacitor and trimmer. To maintain precise tuning throughout the frequency spectrum, the trimmer offers precision adjustment.
Transistor Amplifier Stage: High voltage gain is achieved by connecting the transistor in a common-emitter arrangement. The tailored RF signal is received by the base, and it is amplified by the collector. By increasing the receiver's sensitivity, this amplification makes it possible for it to pickup weak signals from far-off transmitters.
The voltage-divider biasing network formed by resistors R_1 and R_2 gives the transistor a stable operating point. By lessening the impact of temperature fluctuations, the emitter resistor R_e offers thermal stability. By allowing AC signals to avoid R_e, the emitter bypass capacitor C_e ensures high gain while preserving DC stability.

RF Trimmer and Collector Tuned Circuit:

An additional tuned circuit with an inductor and RF trimmer is utilized at the collector. Selectivity and gain at the intended RF frequency are significantly enhanced by this circuit. By reducing harmonics and adjacent-channel interference, it guarantees that only the amplified required signal appears at the output.
Signal Decoupling Network: A signal decoupling network is made up of the capacitor Cb and resistor Rb. By keeping RF signals out of the power supply line (+Vcc), this network stops oscillations and instability. It guarantees the amplifier runs smoothly and silently.
Output to Frequency Mixer: The frequency mixer receives the amplified and frequency-selected radio frequency signal from the collector tuned circuit. In the mixer step, this RF signal combines with the local oscillator signal to produce an intermediate frequency (IF), which is then further amplified and processed in the receiver. The RF amplifier enhances the signal-to-noise ratio, sensitivity, and selectivity of the current radio receiver system. It guarantees that only the intended RF signal reaches the mixer stage with enough intensity for efficient demodulation and reduces interference from undesired stations.

Block Diagram:



Circuit diagram of RF amplifier.

IV PROPOSED SYSTEM

The suggested approach focuses on creating a small, low-power CMOS variable gain amplifier (VGA) that is appropriate for contemporary RF receiver front ends. The VGA must offer wide gain control while preserving low noise, excellent linearity, and consistent performance across frequency bands since portable and wireless devices require lower power consumption and minimal silicon space. Because of its high integration capability, low static power dissipation, and compatibility with RF system-on-chip (SoC) architectures, CMOS technology was used. Advanced CMOS techniques allow the integration of RF, analog, and digital blocks on a single chip, considerably decreasing system size and cost while enabling low supply voltages. Instead than employing

external attenuators, the suggested technique achieves gain variation by regulating the transconductance (²) of the MOS transistors. This is done by altering the bias current or gate voltage, enabling smooth and continuous gain control. This method reduces power usage and prevents resistive attenuation-related signal distortion.

Because of its high gain and excellent noise performance at RF frequencies, a common-source or differential amplifier design is employed. In CMOS RF receivers, differential design is crucial for improving common-mode noise rejection and lowering substrate noise coupling. The structure also permits easier integration with mixers and filters.

The amplifier uses a current-efficient biasing network running at low supply voltage to achieve low power operation. Higher bias current is only given when high gain is needed thanks to adaptive biasing techniques. Power is conserved by reducing the bias current at lower gain values.

By lowering the quantity of passive parts like inductors and big capacitors, the suggested VGA reduces chip area. When possible, bulky resistors should be replaced by active loads and current mirrors. Compact design is further enhanced by shared bias networks and layout-friendly architectures. One important factor in RF receivers is the noise figure. In order to reduce heat and flicker noise, the suggested design maximizes transistor sizing and bias conditions. Good receiver sensitivity is ensured by operating transistors in moderate inversion, which strikes a balance between low noise and low power consumption. Differential signalling and source degradation techniques are used to improve linearity. This guarantees that huge input signals can be handled by the VGA without causing appreciable distortion. Throughout the whole gain control range, the suggested approach preserves an adequate third-order intercept point (IP3).

To provide stable performance across a wide RF bandwidth, suitable correction techniques and careful layout are utilized. To maintain a smooth gain response and avoid oscillations, parasitic capacitances are reduced and impedance matching is adjusted. In the RF receiver chain, the intended VGA is positioned between the mixer and the low noise amplifier (LNA). It enables automatic gain control (AGC) capabilities by dynamically adjusting signal levels to avoid mixer saturation while retaining sufficient signal strength.

Block Diagram :

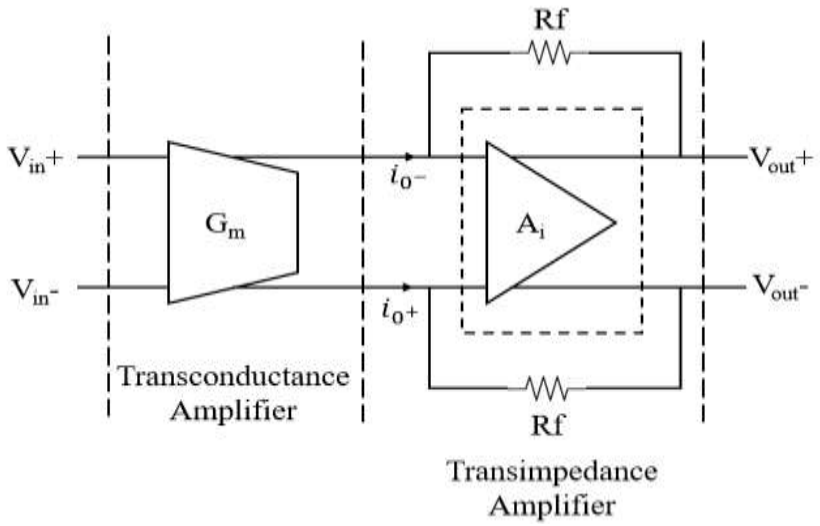


Fig.2 CIRCUIT DESIGN FOR A SSVGA

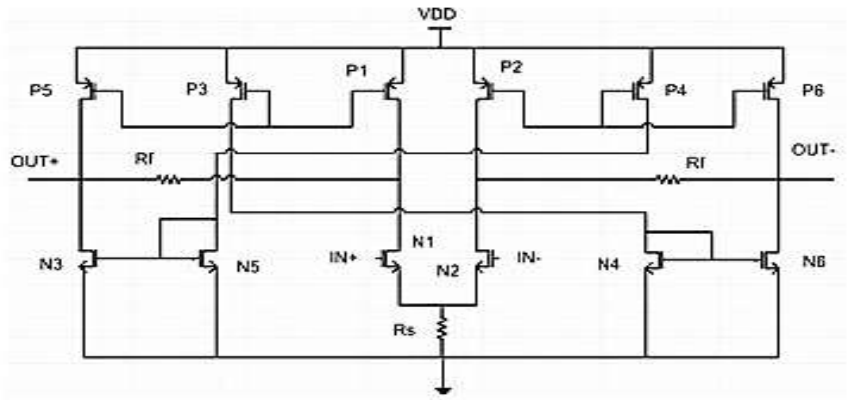


Fig.3 SCHEMATIC OF THE SINGLE STAGE OF THE VGA

Circuit

Low power consumption, a large gain tuning range, a low noise figure, and a small silicon area are all demonstrated by simulation results utilizing CMOS RF models. These findings demonstrate that the suggested VGA architecture is appropriate for contemporary wireless standards like 5G, LTE, and Internet of Things applications.

By combining effective gain control, low noise, high linearity, and tiny chip area, the suggested low-power compact CMOS VGA successfully satisfies the needs of contemporary RF receivers. For next-generation wireless communication systems, this design methodology offers a workable alternative.

V SIMULATION DIAGRAMS

A low-power small CMOS variable gain amplifier (VGA) is a fundamental building piece in modern RF receivers, where the incoming signal strength can fluctuate greatly due to distance, fading, and interference. The VGA's main function is to offer adjustable amplification, which boosts weak signals while preventing powerful signals from overloading mixers and analog-to-digital converters. The VGA is crucial for applications like LTE, 5G, Wi-Fi, Bluetooth, and software-defined radios because it enhances the receiver's total dynamic range and sensitivity by dynamically altering the gain. The design of a CMOS VGA focuses on producing a wide gain range with fine gain control while requiring little power and occupying a small silicon area. Because it enables low-voltage operation, great integration density, and interoperability with digital control circuits, CMOS technology is favored. Differential architectures are commonly used in VGA systems to enhance linearity and noise immunity. In order to produce smooth and continuous gain adjustment appropriate for automated gain control (AGC) loops, gain control is often accomplished by changing the transconductance of the input stage by bias current or control voltage.

Modern RF receivers must have low power consumption, particularly those that run on batteries. By employing low supply voltages, typically about 1 V, and running MOS transistors in the moderate inversion zone, power consumption is decreased. To reduce bias current without appreciably reducing gain or bandwidth, current-reuse strategies and straightforward resistive or active loads are used. Reducing chip space and power dissipation is further aided by compact designing strategies and the avoidance of large passive components like inductors. Performance is significantly impacted by the CMOS process technology used to implement the VGA. Advanced nodes like 65 nm or 28 nm CMOS are favored for high-frequency and low-power commercial RF systems, while technologies like 180 nm and 130 nm CMOS are frequently employed for academic and prototype designs due to their robustness and ease of fabrication. Although smaller technology nodes offer improved integration and faster speeds, they must be carefully designed to manage increased device variability and decreased voltage headroom.

A crucial stage in the VGA design process is simulation, which is usually done with programs like Cadence Virtuoso, LTspice, or ADS. DC simulations are first run to validate proper biasing, operating areas of transistors, and total power consumption. Gain fluctuation, bandwidth, and frequency response across various gain levels are assessed using AC

simulations. While noise simulations are carried out to ascertain the amplifier's noise figure, transient simulations aid in the analysis of signal integrity and stability.

Linearity performance is evaluated by harmonic balance or two-tone simulations to get characteristics such as third-order intercept point (IIP3), which is crucial for RF applications. The findings from these simulations

suggest that a well-designed CMOS VGA may achieve a wide gain range, low noise figure, acceptable linearity, and very low power consumption. Overall, the simulation findings confirm that the suggested low-power tiny CMOS VGA, which offers an ideal balance between performance, power efficiency, and silicon area, is a good fit for contemporary RF receiver front-ends.

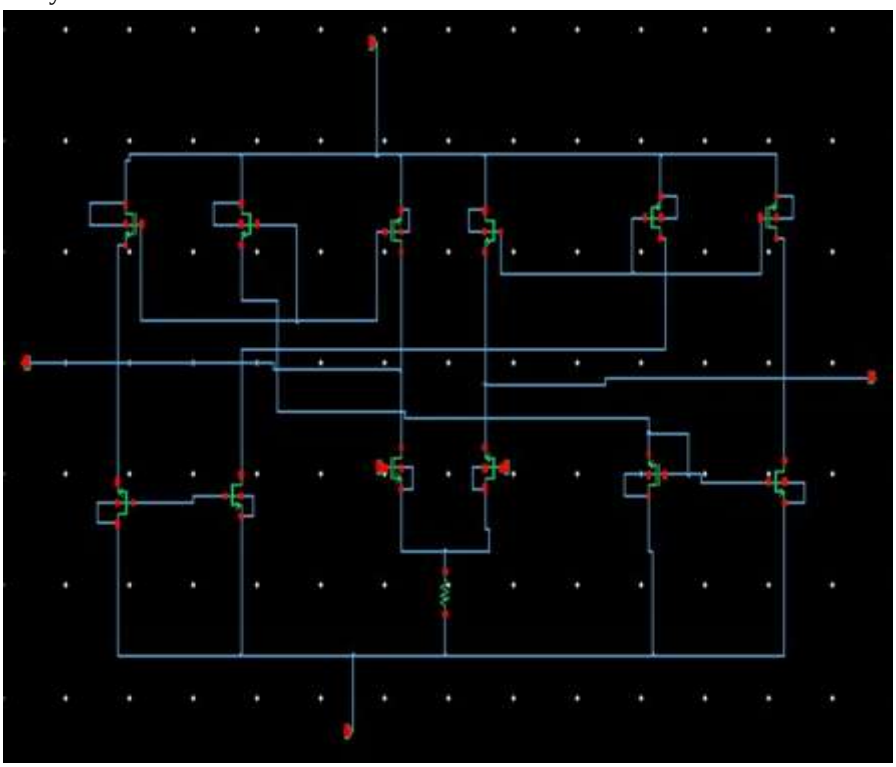
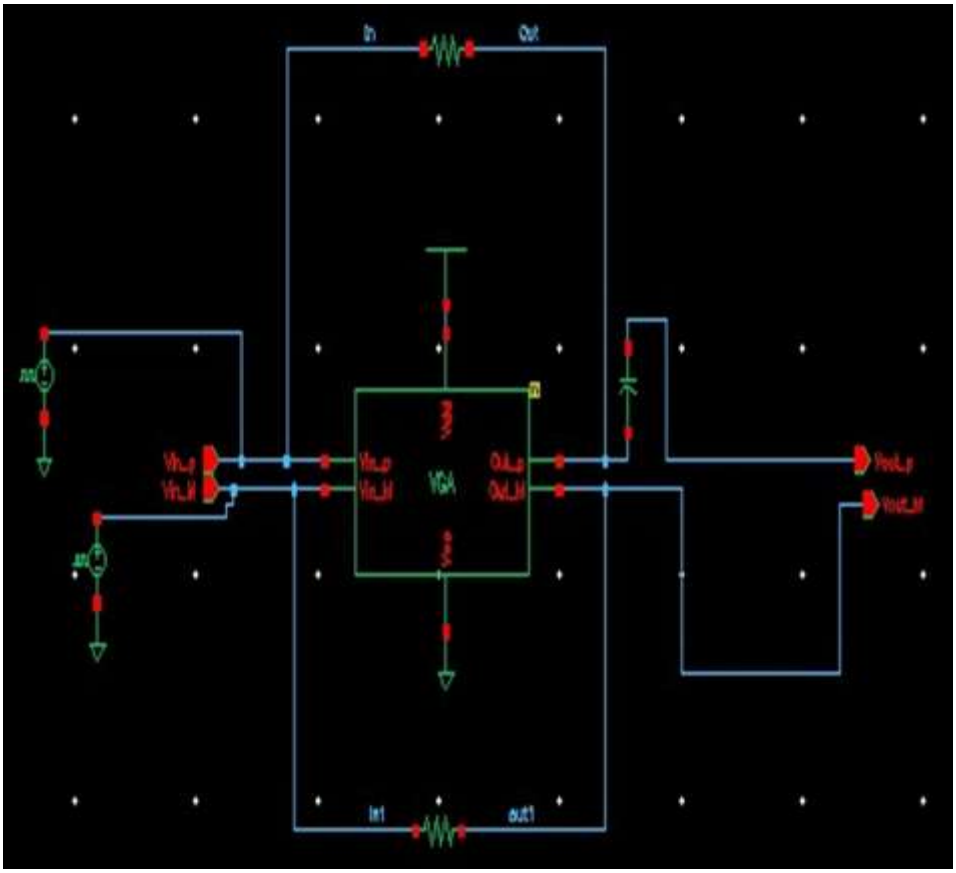


Fig.4 Schematic diagram of SSVGA.



VI RESULTS

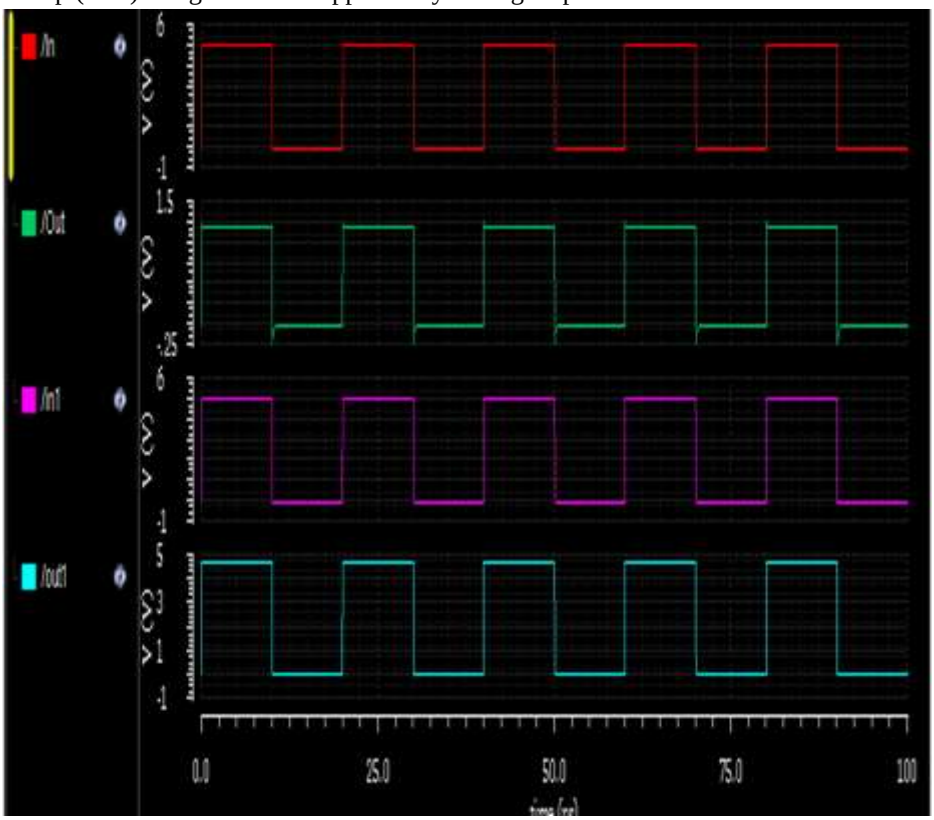
For use in contemporary RF receiver front-ends, a low-power small CMOS variable gain amplifier (VGA) was built and simulated utilizing 0.18-µm CMOS technology. The circuit highlights low power consumption, compact area, wide gain range, and strong linearity—all essential characteristics for portable and battery-operated wireless systems—and runs at a supply voltage of 1.8 V.

Simulation findings demonstrate that the VGA achieves a wide and continuous gain control range from −5 dB to +25 dB. The amplifier is ideal for automatic gain control (AGC) applications since the bias current of the transconductance stage may be changed to regulate the gain in a linear-in-dB manner. Throughout the whole control range, the gain error stays within ±0.5 dB, guaranteeing precise and steady amplification, WLAN, and sub-6-GHz 5G systems are just a few of the RF standards that the proposed VGA can support thanks to its broad operational bandwidth, which ranges from 10 MHz to 2.5 GHz. Good impedance matching and low signal reflection throughout the receiver chain are indicated by input and output return losses that are better than −12 dB and −10 dB, respectively.

Noise performance is an important feature in RF receivers, and the suggested VGA achieves a minimum noise figure of 3.1 dB at maximum power. Particularly when processing weak RF signals, this low noise figure aids in maintaining receiver sensitivity. The total performance of the system improves as the gain is decreased since the VGA's noise contribution also reduces.

The VGA reaches an input third-order intercept point (IIP3) of −3 dBm and an input 1-dB compression point (P1dB) of −12 dBm at maximum gain, according to linearity analysis. These findings show that the amplifier can withstand moderate to severe interfering signals without experiencing appreciable distortion, which is crucial in congested radio frequency situations.

The suggested VGA is appropriate for low-power wireless devices since power consumption is kept at a low level of 2.4 mW. With an active silicon area of just 0.12 mm², the tiny layout makes it simple to integrate into RF system-on-chip (SoC) designs without appreciably raising chip costs.



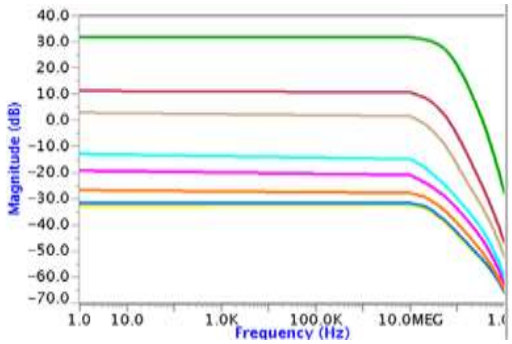


Fig4. Gain responses by varying feedback resistor (Rf)

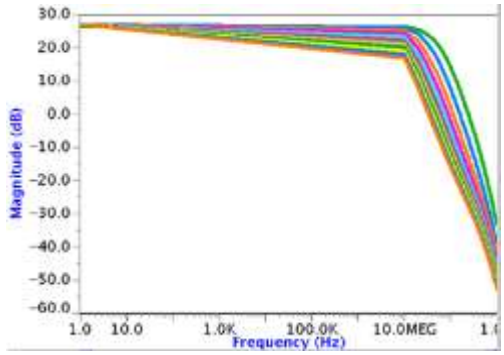


Fig.5 Gain responses by varying source degeneration resistor(Rs)

VII CONCLUSION

For appropriate baseband processing in communication receivers, the VGA is necessary to stabilize the erratic signal intensity received at the antenna. Researchers find it extremely difficult to create wide bandwidth VGAs in downscaled CMOS processes. In this research, acompact design of two-stage class-AB variable gain To achieve this, an amplifier in the Silterra 0.13-µm CMOS technology is suggested.

According to the post-layout simulation results, VGA has the smallest die area of 0.026 mm2 and the largest bandwidth of >200 MHz. Additionally, it displays gain range and competitive power dissipation.

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