

A Flip-Flop Clock Gated 16-Bit Synchronous Gray Code Counter Architecture for Constant Rate High-Speed Counting

1st Mrs. V. Priyadarshini
Electronics and Communication
Engineering
Seshadri Rao Gudlavalleru
Engineering College
Gudlavalleru, India
darshiniv708@gmail.com

2nd Nethala. Durga Devi
Electronics and Communication
Engineering
Seshadri Rao Gudlavalleru
Engineering College
Gudlavalleru, India
nethaladurgadevi13@gmail.com

3rd Shaik. Nasreen Chandini
Electronics and Communication
Engineering
Seshadri Rao Gudlavalleru
Engineering College
Gudlavalleru, India
chandinisyed33@gmail.com

4th Veenam. Geetha kumari
Electronics and Communication
Engineering
Seshadri Rao Gudlavalleru
Engineering College
Gudlavalleru, India
geethakumariveenam@gmail.com

5th Vinukonda. Vikram
Electronics and Communication
Engineering
Seshadri Rao Gudlavalleru
Engineering College
Gudlavalleru, India
vikramvinukonda9@gmail.com

Abstract—This paper presents the design of a high-speed 16-bit synchronous Gray code counter with a constant counting rate, aimed at overcoming the performance degradation observed in conventional binary counters as bit-width increases. The proposed architecture employs a pre-scaled counter structure that maintains a uniform counting rate independent of counter size. An early state detection mechanism reduces critical path delay by enabling faster generation of control signals for subsequent sub-counters. Johnson counters replace traditional T flip-flops, reducing propagation delay and improving operating speed. A flip-flop-based clock gating technique selectively activates the clock only when required, thereby reducing unnecessary switching activity and dynamic power consumption without compromising speed. Results on Xilinx Artix-7 FPGA demonstrate 91.8% total power reduction (0.131 W vs. 1.6 W) and near-complete elimination of dynamic power (<0.001 W), with improved junction temperature (25.2°C vs. 28.0°C), making the design suitable for high-speed digital applications including frequency dividers, phase-locked loops, and IoT-based systems.

Index Terms—Gray code counter; constant time counter; high-speed counter; pre-scaled counter; flip-flop based clock gating; FPGA; Xilinx Artix-7; dynamic power reduction; Johnson counter; synchronous design.

I. INTRODUCTION

In digital circuit design, counters are essential components for applications including time division, synchronization, frequency division, and digital signal processing. However, as the bit-width of counters increases, performance degrades due to increased signal propagation delays through carry chain logic. The High-Speed 16-bit Synchronous Gray Code Counter with Constant Counting Rate addresses this fundamental limitation by ensuring high-speed operation and maintaining a constant counting rate regardless of the number of bits, making it ideal for high-performance and time-sensitive applications [16].

The key design challenges in wide counters are: (1) carry propagation delay growing linearly with bit-width [14]; (2) fan-out overload on pre-scaled enable (PEN) signals driving multiple sub-blocks [9]; (3) setup time constraints of T flip-flops limiting maximum operating

frequency [15]; and (4) excessive dynamic power from always-active clock networks [12]. This work addresses all four challenges simultaneously through a hierarchical Gray code counter architecture with flip-flop-based clock gating.

A. Key Design Features

- **Constant Counting Rate:** Pre-scaling, early state detection, and optimized sub-counter architecture maintain a constant counting rate independent of bit-width [16].
- **High-Speed Operation:** Johnson counter sub-blocks replace T flip-flops, reducing delay and enabling operation in frequency synthesis and PLLs [1], [3].
- **Scalable Architecture:** Hierarchical C₁-C₂-C₃ sub-counter structure scales to 8-bit, 16-bit, and larger configurations without significant performance loss [7].
- **Error Compensation:** Integrated error compensation ensures accuracy in approximation-based high-speed counting, critical for error-resilient applications [11].

II. RELATED WORK

A 0.045–2.5 GHz frequency synthesizer using TDC-based AFC and phase switching multi-modulus divider achieving –120 dBc/Hz phase noise at 1 MHz offset was presented by Hu et al. [1]. This work motivates high-speed counter requirements in frequency synthesis front-ends.

A high-speed digital CMOS divide-by-N frequency divider optimizing speed-power trade-offs in synchronous digital systems was introduced by Abdel-Hafeez et al. [2]. A calibration-free 12 GHz all-digital PLL achieving 78 MHz/μs chirp slope for FMCW radar was demonstrated by Shen et al. [3], establishing stringent counter performance benchmarks for PLL applications.

A CMOS pixel with embedded ADC, digital CDS, and gain correction for massively parallel imaging arrays was developed by Klosowski et al. [4]. A CMOS SPAD sensor with multi-event folded flash TDC for ultra-fast optical transient capture was presented by Al Abbas et al. [5], both requiring precise high-speed counters for timing measurements.

Efficient probabilistic counter-based broadcasting for low-power and lossy IoT networks was proposed by Fedila and Khaoua [6]. Parallel counter implementations for VLSI signal processing achieving high throughput through concurrent operations were analyzed by Jones and Swartzlander [7]. Efficient Hamming weight comparators using accumulative parallel counters were developed by Parhami [8]. Programmable modulo-K counter architectures enabling flexible frequency division were introduced by Lutz and Jayasimha [9].

Systolic frequency dividers/counters enabling high-throughput pipelined implementations were demonstrated by Pekmestzi and Thanasouras [10]. A comparison of binary and LFSR counters with efficient LFSR decoding algorithms was provided by Ajane et al. [11]. Multistage LFSR counters with reduced decoding logic in 130 nm CMOS for large-scale arrays were developed by Morrison et al. [12]. A high-speed counter with novel LFSR state extension achieving superior frequency performance was presented by Bae et al. [13]. Low-power CMOS synchronous counters with clock gating embedded into carry propagation were proposed by Kim et al. [15]. The baseline high-speed synchronous binary counter with constant counting rate is from Kim et al. [16].

III. EXISTING METHOD

Pre-scaled counters divide the counter into smaller sub-blocks, each operating at a lower frequency. The low-order sub-block generates a pre-scaled enable (PEN) signal that activates higher-order sub-blocks. This provides a consistent counting rate where the overall speed is determined by the low-order block operating at the highest frequency [16]. By reducing the frequency of higher-order sub-blocks, delays are minimized and performance is maintained in large-scale systems.

Despite these advantages, pre-scaled counters have significant challenges. The most critical is the fan-out problem: as counter size increases, the PEN signal from the low-order sub-block must drive multiple flip-flops in higher-order sub-blocks, increasing delay with counter size [9]. Ring counters, used to generate the PEN signal, significantly increase hardware complexity. Johnson counters alleviate the fan-out problem through a shift-register state sequence, reducing the number of flip-flops driven by the PEN signal [7]. However, many designs still rely on T flip-flops, which introduce high setup times that limit the maximum operating frequency [14].

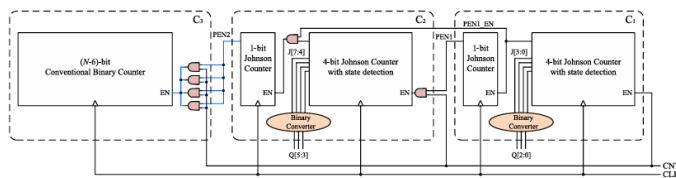


Fig. 1. Existing High-Speed 16-Bit Synchronous Binary Counter with Constant Counting Rate.

As shown in Fig. 1, the existing architecture consists of a conventional (N-6)-bit binary counter (C_1) that generates PEN signals through 1-bit and 4-bit Johnson counters with state detection. Binary converters decode the Johnson counter output to binary form for the counting process. While the combination of Johnson counters and early state detection minimizes delays compared to pure binary counters, three key disadvantages remain.

A. Disadvantages of Existing Method

- **Hardware Complexity:** Multiple flip-flops and logic gates are required to generate PEN1 and PEN2 enable signals. As the counter grows, complexity increases, leading to higher area consumption and power dissipation [12].

- **Power Consumption:** Sequential Johnson counter operation and always-active clock network result in total power of 1.6 W with dynamic power of 1.465 W (92%), dominated by I/O switching (1.377 W, 94%) [15].
- **Limited Scalability:** Maintaining precise PEN signal timing becomes increasingly challenging for very high-speed or large bit-width counters, causing performance degradation in high-frequency applications [16].

IV. PROPOSED METHOD

A. Clock Gating Motivation

Reduction in power dissipation is an essential design issue in VLSI circuits. The clock network is a major source of dynamic power, typically accounting for 30–40% of total dynamic power in synchronous designs. Gating the clock whenever it is not required can significantly reduce switching activity. The proposed design focuses on dynamic power dissipation, reduced by minimizing signal transitions through flip-flop-based clock gating rather than conventional latch-based or combinational AND-gate approaches [15].

B. Flip-Flop Based Clock Gating Cell

In many applications, latch-based designs have been replaced by flip-flop-based designs for improved glitch suppression. By splitting a master-slave flip-flop, two latches can be derived. The flip-flop-based clock gating cell combines a D flip-flop with an AND gate as shown in Fig. 2. This eliminates glitches on the gated clock—unlike a raw AND gate—preventing spurious transitions that would waste power.

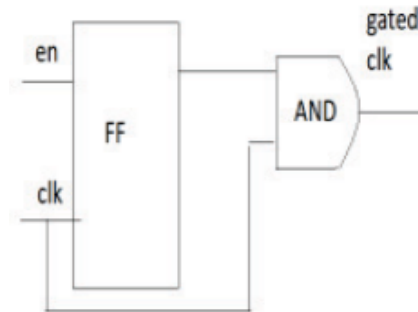


Fig. 2. Block Diagram of Flip-Flop Based Clock Gating Cell (D FF + AND gate).

C. Overall Proposed Architecture

The proposed design is a 16-bit pre-scaled synchronous counter divided into three cascaded sub-counter blocks — C_1 , C_2 , and C_3 — operating on a hierarchical enable chain. A Flip-Flop Based Clock Gating unit controls clock delivery to the entire counter as the primary power reduction technique, as shown in Fig. 3.

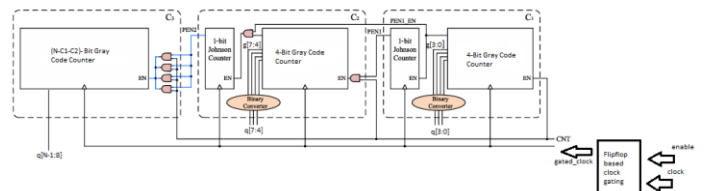


Fig. 3. Proposed 16-bit Flip-Flop Clock Gated Gray Code Counter Architecture.

D. Sub-Counter Block Architecture

C_1 — Bits [3:0], LSB Block

C_1 contains a 4-bit Gray Code Counter (replacing the previous 4-bit Johnson Counter). It counts on every active clock cycle and generates

PEN1 — a pre-scaled enable pulse fired once every 16 clock cycles. PEN1_EN is forwarded to C₂ to trigger its counting.

C₂ — Bits [7:4], Middle Block

C₂ contains a 4-bit Gray Code Counter plus a 1-bit Johnson Counter for state detection. It is enabled only when PEN1 from C₁ is asserted (every 16 cycles), generating PEN2 once every 256 clock cycles. A Binary Converter decodes the Gray output to binary q[7:4].

C₃ — Bits [15:8], MSB Block

C₃ contains an (N-C₁-C₂)-bit Gray Code Counter, enabled only when PEN2 from C₂ is asserted (every 256 cycles). A 1-bit Johnson Counter provides early terminal state detection. Outputs the upper binary bits q[N-1:8].

E. Power Reduction Mechanism

The CNT (count enable) signal and system clock are fed into the Flip-Flop Based Clock Gating cell, producing a gated_clock delivered to all three sub-counter blocks. When enable = 0, gated_clock is suppressed — all flip-flops freeze and zero dynamic switching power is consumed. When enable = 1, normal counting resumes. The flip-flop stage eliminates glitches on the gated clock, preventing spurious transitions that would waste power. This is the most impactful power saving technique in the proposed design.

F. Advantages of Proposed Method

- **Reduced Power:** 0.131 W total vs. 1.6 W (91.8% reduction). Dynamic power reduced to <0.001 W through selective clock gating that eliminates unnecessary switching activity.
- **Improved Speed:** Flip-flop-based clock gating reduces clock load, decreasing setup time issues. Flip-flops switch only when needed, optimizing overall performance.
- **Reduced Hardware Complexity:** Selective clock operation reduces the need for extra logic gates compared to traditional pre-scaling and enable generation methods.
- **Scalability:** Inactive sub-blocks during clock gating reduce overall system complexity and maintain performance across wider bit-width configurations.

V. APPLICATIONS

A. High-Frequency Signal Processing

In frequency synthesizers, phase-locked loops (PLLs), and digital clocks, counters divide the frequency of incoming signals to lower frequencies [1], [3]. The proposed design's low power consumption and efficient counting mechanism ensure stable operation where traditional counters may struggle with speed and power.

B. Embedded Systems and IoT Devices

Microcontrollers and embedded systems rely on efficient timers and counters for interval measurement, periodic signal generation, and PWM control [6]. The flip-flop clock gating enables long battery life while maintaining high performance in wearable devices, smart sensors, and low-power IoT nodes.

C. Digital Signal Processors

DSPs for audio/video processing, telecommunications, and radar use high-speed counters in digital filtering and FFT algorithms. The proposed counter's improved speed and reduced power suit portable processing systems where throughput and energy efficiency are simultaneously critical [5].

D. Communication Systems and Real-Time Clocks

In 5G networks, satellite communications, and data encoding applications, pre-scaled counters generate precise timing signals and

manage multiple data streams [2]. The reduced dynamic power makes the design particularly valuable in battery-operated real-time clock circuits for GPS systems and wearable devices.

VI. RESULTS AND DISCUSSION

The proposed 16-bit flip-flop clock gated Gray code counter was implemented in Verilog HDL and synthesized on Xilinx Artix-7 FPGA. Functional verification was performed through simulation, and power analysis was conducted using Vivado power estimation from synthesized netlist with activity derived from simulation files.

A. Simulation Waveform

Fig. 4 shows the simulation waveform of the proposed high-speed 16-bit Gray code counter with flip-flop based clock gating, confirming correct Gray code counting sequence with hierarchical enable signal generation (PEN1 every 16 cycles, PEN2 every 256 cycles) and proper gated clock behavior.

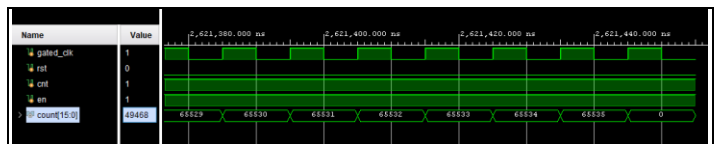


Fig. 4. Simulation Waveform of Proposed High-Speed 16-bit Gray Code Counter with Flip-Flop Based Clock Gating.

B. Power Analysis

Fig. 5 presents the on-chip power analysis from Xilinx Vivado for the existing design and Fig. 6 presents the on-chip power analysis from Xilinx Vivado for the proposed design. Total on-chip power is 0.131 W, dominated by device static power (99%), confirming near-complete elimination of dynamic switching activity through effective clock gating.

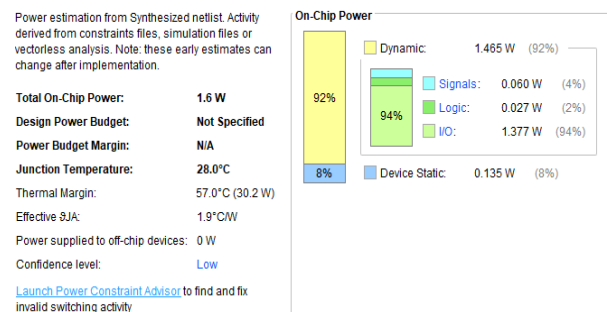


Fig. 5. On-Chip Power Analysis of Existing High-Speed 16-Bit Synchronous Binary Counter with Constant Counting Rate

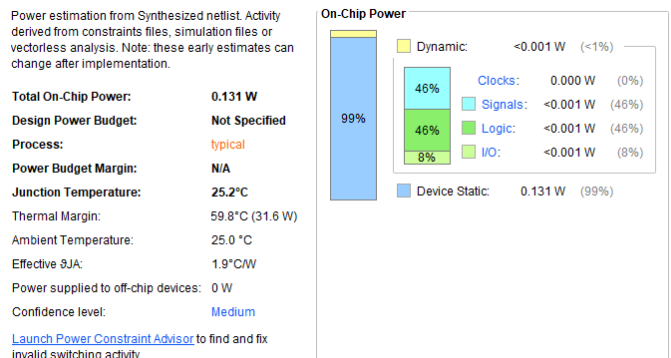


Fig. 6. On-Chip Power Analysis of Proposed Flip-Flop Clock Gated Gray Code Counter (Xilinx Artix-7).

C. Comparison with Existing Method

Table 1 presents a comprehensive comparison between the existing method [16] and the proposed optimized clock gated Gray code counter. The proposed design achieves 91.8% total power reduction, near-complete elimination of dynamic power (~99.9%), and improved thermal margin, confirming the effectiveness of flip-flop based clock gating with Gray code counter architecture.

Table 1. Power Comparison: Existing Method [16] vs. Proposed Optimized Gray Code Counter.

Parameter	Existing [16]	Proposed	Reduction
Total On-Chip Power (W)	1.6	0.131	91.8%
Dynamic Power (W)	1.465 (92%)	<0.001 (<1%)	~99.9%
Device Static Power (W)	0.135 (8%)	0.131 (99%)	~3%
Signals Power (W)	0.060 (4%)	<0.001 (46%)	~98%
Logic Power (W)	0.027 (2%)	<0.001 (46%)	~96%
I/O Power (W)	1.377 (94%)	<0.001 (8%)	~99.9%
Junction Temperature (°C)	28.0	25.2	↓ 2.8°C
Thermal Margin (°C / W)	57.0°C (30.2 W)	59.8°C (31.6 W)	↑ Improved

The drastic reduction in dynamic power from 1.465 W to <0.001 W represents the core contribution of flip-flop based clock gating: when counting is not required (enable = 0), the gated_clock suppresses all flip-flop transitions, eliminating virtually all dynamic switching activity. The marginal reduction in device static power (0.135 W → 0.131 W) confirms that static leakage is unaffected by clock gating — only dynamic switching is controlled. The improved junction temperature (25.2°C vs. 28.0°C) and expanded thermal margin confirm better thermal management of the proposed design.

VII. CONCLUSION

This paper presented a flip-flop clock gated 16-bit synchronous Gray code counter architecture for constant rate high-speed counting. The proposed design integrates flip-flop-based clock gating into a hierarchical pre-scaled Gray code counter (C₁-C₂-C₃) to simultaneously address power consumption, operating speed, hardware complexity, and scalability limitations of existing counter designs [16].

FPGA implementation on Xilinx Artix-7 demonstrates 91.8% total power reduction (0.131 W vs. 1.6 W), near-complete elimination of dynamic power (<0.001 W from 1.465 W), and improved junction temperature (25.2°C). The hierarchical C₁-C₂-C₃ sub-counter structure with Gray code counting, Johnson counter state detection, and flip-flop gated clock delivery provides a scalable, power-efficient solution for high-speed digital applications including frequency synthesizers, PLLs, IoT edge nodes, and digital signal processors.

Future work will explore extension to 32-bit and 64-bit configurations, integration with adaptive voltage scaling for further power reduction, and evaluation under varying environmental conditions and data rates to fully characterize bit error rates in communication applications.

ACKNOWLEDGMENT

The authors thank the Department of Electronics and Communication Engineering, Mother Theresa Institute of Engineering and Technology (MIET), Palamaner, affiliated to Jawaharlal Nehru Technological University Anantapur (JNTUA), for providing the necessary resources, infrastructure, and FPGA development tools for this research.

REFERENCES

[1] A. Hu, D. Liu, K. Zhang, L. Liu, and X. Zou, "A 0.045- to 2.5-GHz frequency synthesizer with TDC-based AFC and phase switching multi-modulus

divider," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 12, pp. 4470–4483, Dec. 2020. DOI: <https://doi.org/10.1109/TCSI.2020.3020761>

[2] S. Abdel-Hafeez, S. M. Harb, and W. R. Eisenstadt, "High speed digital CMOS divide-by-N frequency divider," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2008, pp. 592–595. DOI: <https://doi.org/10.1109/ISCAS.2008.4541487>

[3] Z. Shen et al., "A 12 GHz calibration-free all-digital PLL for FMCW signal generation with 78 MHz/μs chirp slope and high chirp linearity," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 12, pp. 4445–4456, Dec. 2020. DOI: <https://doi.org/10.1109/TCSI.2020.3004363>

[4] M. Klosowski, W. Jendernalik, J. Jakusz, G. Blakiewicz, and S. Szczepanski, "A CMOS pixel with embedded ADC, digital CDS, and gain correction capability for massively parallel imaging array," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 1, pp. 38–49, Jan. 2017. DOI: <https://doi.org/10.1109/TCSI.2016.2610524>

[5] T. Al Abbas et al., "A CMOS SPAD sensor with a multi-event folded flash time-to-digital converter for ultra-fast optical transient capture," IEEE Sensors J., vol. 18, no. 8, pp. 3163–3173, Apr. 2018. DOI: <https://doi.org/10.1109/JSEN.2018.2803087>

[6] D. A. Fedila and M. O. Khaoua, "Efficient probabilistic counter-based broadcast for low-power & lossy networks," in Proc. Int. Conf. Adv. Electron., Control Commun. Syst. (ICAECSS), Mar. 2023, pp. 1–6. DOI: <https://doi.org/10.1109/ICAECSS56710.2023.10105089>

[7] R. F. Jones and E. E. Swartzlander, "Parallel counter implementation," J. VLSI Signal Process. Syst. Signal, Image Video Technol., vol. 7, no. 3, pp. 223–232, Oct. 1994. DOI: <https://doi.org/10.1007/BF02409399>

[8] B. Parhami, "Efficient Hamming weight comparators for binary vectors based on accumulative and Up/Down parallel counters," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 2, pp. 167–171, Feb. 2009. DOI: <https://doi.org/10.1109/TCSII.2008.2010176>

[9] D. R. Lutz and D. N. Jayasimha, "Programmable modulo-K counters," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 43, no. 11, pp. 939–941, Nov. 1996. DOI: <https://doi.org/10.1109/81.542285>

[10] K. Z. Pekmestzi and N. Thanasouras, "Systolic frequency dividers/counters," IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process., vol. 41, no. 11, pp. 775–776, Nov. 1994. DOI: <https://doi.org/10.1109/82.331551>

[11] A. Ajane, P. M. Furth, E. E. Johnson, and R. L. Subramanyam, "Comparison of binary and LFSR counters and efficient LFSR decoding algorithm," in Proc. IEEE 54th Int. Midwest Symp. Circuits Syst. (MWSCAS), Aug. 2011, pp. 1–4. DOI: <https://doi.org/10.1109/MWSCAS.2011.6026392>

[12] D. Morrison, D. Delic, M. R. Yuce, and J.-M. Redouté, "Multistage linear feedback shift register counters with reduced decoding logic in 130 nm CMOS for large-scale array applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 27, no. 1, pp. 103–115, Jan. 2019. DOI: <https://doi.org/10.1109/TVLSI.2018.2872021>

[13] H. Bae et al., "High-speed counter with novel LFSR state extension," IEEE Trans. Comput., vol. 72, no. 3, pp. 893–899, Mar. 2023. DOI: <https://doi.org/10.1109/TC.2022.3187343>

[14] P. Larsson and J. Yuan, "Novel carry propagation in high-speed synchronous counters and dividers," Electron. Lett., vol. 29, no. 16, pp. 1457–1458, Aug. 1993. DOI: <https://doi.org/10.1049/el:19930972>

[15] Y.-W. Kim et al., "Low-power CMOS synchronous counter with clock gating embedded into carry propagation," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 8, pp. 649–653, Aug. 2009. DOI: <https://doi.org/10.1109/TCSII.2009.2025627>

[16] S. Kim, J. Kim, and I.-C. Park, "High-Speed CMOS Synchronous Binary Counter with Constant Counting Rate," IEEE Access, vol. 13, pp. 53347–53355, 2025. DOI: <https://doi.org/10.1109/ACCESS.2025.3553580>